ABSTRACT

A method, for executing a load locked and a store conditional instruction in a processor, achieves an atomic read-write operation to a memory block. First the load locked instruction is executed to read a memory block, and the processor in response to executing the load locked instruction issues a read modify system command to read the block and to take ownership of the block by the processor, and also sets a lock flag for the address of the memory block, and writes a value of the memory block into a cache of the processor as a cache copy of the memory block. The lock flag, upon receipt of an invalidate message by the processor for the cache copy of the memory block, is reset if any invalidate messages for the memory block are received by the processor. The processor waits for a selected time interval before the processor surrenders ownership of the memory block upon receipt of an ownership request message, if any is received by the processor after execution of the load locked instruction. The processor executes the store conditional instruction, and the processor in response to executing the store conditional instruction tests the lock flag, and if the lock flag is set, writing to the cache copy of the memory block. The processor ends, in the event that the lock flag is reset, the store conditional instruction and does not write to the cache copy of the memory block.